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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,457	02/12/2004	Marco Pasotti	S1022.81104US00	2275

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WOLF GREENFIELD & SACKS, P.C.
600 ATLANTIC AVENUE
BOSTON, MA 02210-2206

EXAMINER	
PHAN, TRONG Q	
ART UNIT	PAPER NUMBER
2827	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,457	PASOTTI ET AL.	
	Examiner	Art Unit	
	TRONG PHAN	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 July 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-12* is/are allowed.

6)☒ Claim(s) *13-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 13-26 and 30-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim, 6,445,616.

Kim, 6,445,616, discloses in Fig. 3 a sense amplifier for a memory cell comprising:

Claims 13, 30-31 and 33-36:

a first transistor (NM2) having a first conducting terminal coupled to a reference memory cell (read reference cell RFC) and a second conducting terminal for connection to a supply voltage (VPD via diode-connected transistor MP102); and

a control circuit (950) coupled to a control input of the first transistor (NM2) and the first conducting terminal of the first transistor (NM2) such that the control circuit (950) applies a control voltage (reg2) to the control input of the first transistor in response to a voltage of the first conducting terminal, wherein the control circuit controls the first transistor to provide a reading current to the reference memory cell (read reference cell RFC), wherein the reading current passes through both the reference memory cell and the first transistor at the same time;

Claim 14:

the control circuit (950) comprises a first feedback amplifier (OPA3);

Claims 15-16:

a first input (+) of the feedback amplifier (OPA3) is coupled to a reference voltage (PRBIAS);

Claim 17:

a second input (-) of the first feedback amplifier (OPA3) is coupled to the first conducting terminal;

Claim 18:

an output (reg2) of the first feedback amplifier is coupled to the control input of the first transistor;

Claim 19:

the first transistor is a PMOS transistor;

Claim 20:

a comparator (OPA1) coupled to the first transistor (NM2) and the memory cell (MC) for providing a voltage (SAOUT) representative of data stored in the memory cell (MC);

Claim 21:

a second transistor (NM1) having a first conducting terminal coupled to the memory cell (MC);

Claim 22:

the second transistor has a second conducting terminal coupled to the supply voltage (VPD) and a control input coupled to the control circuit;

Claim 23:

the control circuit comprises a first feedback amplifier (OPA3) coupled to the first transistor (NM2) and a second feedback amplifier (OPA1) coupled to the second transistor (NM1);

Claim 24:

a first input (+) of the second feedback amplifier (OPA1) is coupled to a reference voltage (PRBIAS);

Claim 25:

a second input (-) of the second feedback amplifier (OPA1) is coupled to the first conducting terminal of the second transistor (NM1);

Claim 26:

a comparator (OPA2);

wherein the first feedback amplifier (OPA3) and the second feedback amplifier (OPA1) are coupled to the comparator (OPA2), which provides a voltage (SAOUT) representative of data stored in the memory cell (MC);

Claim 27:

the control circuit comprises a first feedback amplifier (OPA3) coupled to the first transistor (NM2) and the second transistor (NM1);

Claim 32:

the first transistor (NM2) acts as a reference load.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim, 6,445,616, in view of Pasotti et al., 6,535,428.

What is not shown in Fig. 3 of Kim, 6,445,616, is the features recited in claims 28-29.

Pasotti et al., 6,535,428, discloses in Fig. 1 the teaching of using NMOS transistors MN1 connecting load MP1 and memory cells MC and NMOS transistor MN2 connecting between load transistor MP2 and reference memory cells CR. Also, as shown in Fig. 2, each of NMOS transistors MN1 and MN2 is controlled by a feedback inverter INV1 (it should be noted that Fig. 2 does show only circuit branch 11 (see lines 59-65, column 8).

It would have been obvious under 35 USC 103(a) to one of ordinary skill in the art at the time of the present invention was made to utilize a second set of NMOS transistor MN2 and inverter INV1 for coupling to the read reference memory cell RFC in Fig. 3 of Kim, 6,445,616, for the purpose of keeping the drain voltage of the read reference memory cell RFC as a predetermined value (see lines 10-24, column 5 of Pasotti et al., 6,535,428).

Allowable Subject Matter

5. Claims 1-12 are allowed.

6. The following is an examiner's statement of reasons for allowance:

"A sense amplifier for nonvolatile memory cells comprising: a reference cell, a first load for connection between a supply terminal and an input terminal of an output comparator, said first load being connected to said reference cell via a first conduction terminal, and further comprising a second load, connectable to a nonvolatile memory cell, said first load and said second load each having a controllable resistance, and a control circuit controlling said first load and said second load and feeding said first load and said second load with a control voltage independent of an operating voltage between the first conduction terminal and a second conduction terminal of said first load, wherein the first load is controlled by the control circuit in response to a voltage of the first conduction terminal of the first load to provide a reading current to the reference cell during a reading of the nonvolatile memory cell, wherein the reading current passes through both the reference cell and the first load at the same time" recited in claims 1-12 is patentable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to TRONG PHAN whose telephone number is (571) 272-1794. The examiner can normally be reached on M-F (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, AMIR ZARABIAN can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/TRONG PHAN/
Primary Examiner, Art Unit 282799